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AMENDMENTS TO THE CLAIMS:

Please add new claims 36-38 as follows:

1. (Previously Presented) A double-gate field effect transistor, comprising:

a strained-silicon channel formed adjacent a source and a drain;

a first gate formed over a first side of said channel;

a second gate formed over a second side of said channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and

a second gate dielectric formed between said second gate and said strained-silicon channel,

wherein said strained-silicon channel is non-planar.

2. (Previously Presented) The transistor of claim 1, wherein said strained-silicon channel thickness is substantially uniform.

3. (Previously Presented) The transistor of claim 1, wherein said strained-silicon channel thickness is set by epitaxial growth.

4. (Previously Presented) The transistor of claim 1, wherein said strained-silicon channel is substantially defect-free.

5. (Previously Presented) The transistor of claim 1, wherein said strained-silicon channel includes a distorted lattice cell.

6. (Previously Presented) The transistor of claim 1, wherein said first gate and said second gate are independently controllable.

7. (Previously Presented) The transistor of claim 1, wherein said strained-silicon channel comprises a fin.

8. (Previously Presented) The transistor of claim 1, wherein said first gate and said second gate are self-aligned.

9. (Previously Presented) The transistor of claim 1, wherein said first gate and said second gate are defined in a single lithographic step.

10. (Previously Presented) The transistor of claim 1, wherein said first gate, said second gate, said source and said drain are self-aligned with respect to each other.

11. (Previously Presented) The transistor of claim 7, further comprising a plurality of fins.

12. (Previously Presented) The transistor of claim 1, wherein said device includes a planarized top surface.

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Previously Presented) A double-gate field effect transistor, comprising:

a strained-silicon channel formed adjacent a source and a drain;

a first gate formed over a first side of said channel;

a second gate formed over a second side of said channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and a second gate dielectric formed between said second gate and said strained-silicon channel,

wherein said strained-silicon channel comprises a fin.

22. (Previously Presented) A circuit, comprising:

the double-gate field effect transistor of claim 1.

23. (Previously Presented) The transistor of claim 1, wherein said strained-silicon channel is tensely strained.

24. (Previously Presented) The transistor of claim 1, wherein said strained-silicon channel is compressively strained.

25. (Canceled)

26. (Canceled)

27. (Canceled)

28. (Previously Presented) The transistor of claim 1, wherein the first gate is electrically separated from the second gate.

29. (Previously Presented) The transistor of claim 21, wherein the first gate is electrically separated from the second gate.

30. (Previously Presented) A semiconductor device, comprising:

a strained-silicon channel formed adjacent a source and a drain;

a first gate formed over a first sidewall of said channel;

a second gate formed over a second sidewall of said channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and a second gate dielectric formed between said second gate and said strained-silicon channel,

wherein said strained-silicon channel is non-planar, and said first and second sidewalls are opposing to each other.

31. (Previously Presented) A semiconductor device, comprising:

a strained-silicon channel formed adjacent a source and a drain, wherein strain in said strained-silicon channel was elastically induced by a sacrificial stressor;

a first gate formed over a first side of said channel;

a second gate formed over a second side of said channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and a second gate dielectric formed between said second gate and said strained-silicon channel, wherein said strained-silicon channel is non-planar, and is fixed to the substrate by said first and second gates.

32. (Previously Presented) The transistor of claim 1, wherein strain in said strained-silicon channel was elastically induced by a sacrificial stressor.

33. (Previously Presented) The transistor of claim 21, wherein strain in said strained-silicon channel was elastically induced by a sacrificial stressor.

34. (Previously Presented) The transistor of claim 1, wherein said strained-silicon channel is

controlled by said first gate and by said second gate.

35. (Previously Presented) The transistor of claim 21, wherein said strained-silicon channel is controlled by said first gate and by said second gate.

36. (New) The transistor according to claim 1, wherein said first gate and said second gate are separated from one another.

37. (New) The transistor according to claim 1, wherein carriers in said channel are controlled by said first gate and said second gate.

38. (New) The transistor according to claim 1, wherein said channel a first vertical surface covered by said first gate dielectric and a second vertical surface covered by said second gate dielectric.